322 D 7880

THIRD ANGLE PROJECTION

A-GA CONTROL

C6A — MATRIX ADDRESS S2 S4 CA C

OPERATION	WAVE-FORMS	TIMING
Transfer function into J.reg. Set J.reg. with address of B.reg. and then read contents of B.reg. into M.reg.	WRITE	*
	READ	*
	GTQ	T4
	OTQ	T3
	OTJ	T3
	OTM	T3
	MTI	T2
	VTG	T2
	OTI	T1
	OTG	T1
	ETJ	*
	KI	*
	DTF1	*
	MTF	*

C7 — MATRIX ADDRESS S3 S4 C

OPERATION	WAVE-FORMS	TIMING
Add contents of M.reg. and Q.reg. and put result in M.reg. Enable Function Decode.	GTM	T4
	OTM	T3
	OTJ	T3
	FTG	T2
	OTG	T1
	SFD	*
	MTF	*
	QTF	*

C6B — MATRIX ADDRESS S2 S4 $\overline{CA}$ C

OPERATION	WAVE-FORMS	TIMING
Transfer function from M.reg. into I.reg. and enable Function Decode	GTM	T4
	OTM	T3
	OTJ	T3
	MTI	T2
	VTG	T2
	OTI	T1
	OTG	T1
	SFD	*
	DTF1	*
	MTF	*

M18=1 M18=0

C5 — MATRIX ADDRESS S1 S4 C

OPERATION	WAVE-FORMS	TIMING
Test for B modifier and set J.reg to zero.		
	TM18	*

C4 — MATRIX ADDRESS S0 S4 C

OPERATION	WAVE-FORMS	TIMING
Decrease M.reg by 1 then transfer into J.reg. Read contents of that address into M.reg.	WRITE	*
	READ	*
	GTJ	T4
	OTM	T3
	OTJ	T3
	FTG	T2
	OTG	T1
	DTF2	*
	DTF1	*
	MTF	*

C3 — MATRIX ADDRESS S3 $\overline{S4}$ C

OPERATION	WAVE-FORMS	TIMING
Increase M.reg by 1 and rewrite in SCR.	WRITE	*
	GTM	T4
	OTM	T3
	FTG	T2
	OTG	T1
	ITF	*
	MTF	*

C2 — MATRIX ADDRESS S2 $\overline{S4}$ C

OPERATION	WAVE-FORMS	TIMING
Set address of SCR for level selected by interrupt. Read SCR into M.reg.	READ	*
	OTM	T3
	OTJ	T3
	WFR	*
	ETJ	*
	DTE	*

C1A — MATRIX ADDRESS S1 $\overline{S4}$ CA C

OPERATION	WAVE-FORMS	TIMING
Transfer M.reg. into A.reg.	GTA	T4
	OTA	T3
	FTG	T2
	OTG	T1
	MTF	*

NGA

C1B — MATRIX ADDRESS S1 $\overline{S4}$ $\overline{CA}$ C

OPERATION	WAVE-FORMS	TIMING
—	—	—

C0 — MATRIX ADDRESS S0 $\overline{S4}$ C

OPERATION	WAVE-FORMS	TIMING
Transfer word gen. into M. reg. & test NGA. Clear J.reg. & ignore extnl. interrupts.	WTM	T4
	OTM	T3
	OTJ	T3
	TNGA	*
	DTE	*

ENTRY POINT WHEN USING ENTER, OBEY OR JUMP KEYS

A-GB 0 SET B REGISTER

00 — MATRIX ADDRESS S0 $\overline{S4}$ DD DH

OPERATION	WAVE-FORMS	TIMING
Transfer address from M.reg. into J.reg. then read number from that address into M.reg.	MTF	*
	DTF1	*
	DTF2	*
	OTG	T1
	VTG	T2
	OTM	T3
	GTJ	T4
	READ	*
	WRITE	*

01 — MATRIX ADDRESS S1 $\overline{S4}$ DD DH

OPERATION	WAVE-FORMS	TIMING
Set J.reg. with address of present level B.reg. Transfer number from M.reg. into Q.reg. Write number into B.reg.	MTF	*
	ETJ	*
	KI	*
	OTG	T1
	FTG	T2
	OTJ	T3
	OTQ	T3
	GTQ	T4
	CLEAR	*
	WRITE	*

A-GB 1 ADD

10 — MATRIX ADDRESS S0 $\overline{S4}$ DB DH

OPERATION	WAVE-FORMS	TIMING
Transfer address from M.reg. into J.reg. then read number from that address into M.reg.	MTF	*
	DTF1	*
	DTF2	*
	OTG	T1
	VTG	T2
	OTM	T3
	GTJ	T4
	READ	*
	WRITE	*

11 — MATRIX ADDRESS S1 $\overline{S4}$ DB DH

OPERATION	WAVE-FORMS	TIMING
Add contents of A.reg. and M.reg. then place result in A. reg.	MTF	*
	ATF	*
	OTG	T1
	FTG	T2
	OTA	T3
	GTA	T4

A-GC 2 NEGATE AND ADD

20 — MATRIX ADDRESS S0 $\overline{S4}$ DC DH

OPERATION	WAVE-FORMS	TIMING
Transfer address from M.reg. into J.reg. then read number from that address into M.reg.	MTF	*
	DTF1	*
	DTF2	*
	OTG	T1
	VTG	T2
	OTM	T3
	GTJ	T4
	READ	*
	WRITE	*

21 — MATRIX ADDRESS S1 $\overline{S4}$ DC DH

OPERATION	WAVE-FORMS	TIMING
Transfer M.reg. into Q.reg.	MTF	*
	OTG	T1
	FTG	T2
	OTQ	T3
	GTQ	T4

22 — MATRIX ADDRESS S2 $\overline{S4}$ DC DH

OPERATION	WAVE-FORMS	TIMING
Transfer A.reg. into M.reg.	ATF	*
	OTG	T1
	FTG	T2
	OTM	T3
	GTM	T4

23 — MATRIX ADDRESS S3 $\overline{S4}$ DC DH

OPERATION	WAVE-FORMS	TIMING
Add 2's complement of M.reg. to Q.reg. and place result in A.reg.	MTF	*
	ITF	*
	QTF	*
	OTG	T1
	FTG	T2
	OTA	T3
	GTA	T4

A-GB 3 STORE Q REGISTER

30 — MATRIX ADDRESS S0 $\overline{S4}$ DA DH

OPERATION	WAVE-FORMS	TIMING
Transfer address from M.reg. into J.reg. and set overflow unit to zero	MTF	*
	DTF1	*
	DTF2	*
	OTG	T1
	VTG	T2
	OTX	T3
	GTJ	T4

31 — MATRIX ADDRESS S1 $\overline{S4}$ DA DH

OPERATION	WAVE-FORMS	TIMING
Right shift Q.reg by 1 bit whilst transfering it to M.reg Write contents of M.reg. into above address	QTF	*
	XTF	*
	OTG	T1
	RTG	T2
	OTM	T3
	GTM	T4
	CLEAR	*
	WRITE	*

A-GB 4 READ

40 — MATRIX ADDRESS S0 $\overline{S4}$ DD DF

OPERATION	WAVE-FORMS	TIMING
Transfer address from M.reg. into J.reg. then read number from that address into M.reg	MTF	*
	DTF1	*
	DTF2	*
	OTG	T1
	VTG	T2
	OTM	T3
	GTJ	T4
	READ	*
	WRITE	*

41 — MATRIX ADDRESS S1 $\overline{S4}$ DD DF

OPERATION	WAVE-FORMS	TIMING
Transfer M.reg. into A.reg.	MTF	*
	OTG	T1
	FTG	T2
	OTA	T3
	GTA	T4

TO SHEET 2

FROM SHEET 2

* Waveforms set true at T6 of previous timing cycle and set false at T6 of present timing cycle

Note that the waveforms CLEAR, READ, WRITE and some test waveforms (eg. TM_{18}) whilst being set true at T6 of previous timing cycle are not in fact used until T5 of present timing cycle.

TITLE
920 B
CONTROL SEQUENCE.
FUNCTIONS 0-9.

SHEET 1 OF 2

A11

LATEST MI INCORPORATED; MI ~~[illegible]~~ 2998

ISSUE No.	1	2	
ALTN No.	1620	1769	
DATE	25.8.66	23.8.4	
INITIALS	S.N.	[illegible]	
PARTS LIST No.			

DRAWN S.NIBLETT. CHECKED CS.707 APPROVED A.Wood DATE 30-9-66

MATERIAL FINISH

© Elliott Brothers (London) Limited
THIS DRAWING IS THE PROPERTY OF ELLIOTT BROTHERS (LONDON) LIMITED AND MAY NOT BE COPIED USED OR DISCLOSED FOR ANY PURPOSE EXCEPT AS AUTHORISED IN WRITING BY ELLIOTT BROTHERS (LONDON) LIMITED

TOLERANCES
DECIMAL ±
FRACTIONAL ±
ANGULAR DIMENSIONS ±
UNLESS OTHERWISE STATED

ELLIOTT BROTHERS (LONDON) LTD

TITLE 920 B CONTROL SEQUENCE. FUNCTIONS 0-9.

SHEET 1 OF 2

DRAWING No. 322 D 7880